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Efficient **instruction encoding** for automatic **instruction** set design of configurable ASIPs- ▶psu.edu [PDF]
J Lee, K Choi, N Dutt - Proceedings of the 2002 IEEE/ACM international conference on ..., 2002 - portal.acm.org
**...** vary among instructions to allow more compact **encoding** of the **...** while it may have 8
bits in an ADDI **instruction**. **Register** fields can also have a reduced size to **...**
Cited by 43 - Related articles - Web Search - BL Direct - All 15 versions

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R Mehta, RM Owens, MJ Irwin, R Chen, D Ghosh, E ... - Low Power Electronics and Design, 1997. Proceedings., 1997 ..., 1997 - ieeexplore.ieee.org
**...** This includes all switching in the **instruction register** and decoder due to changes
in **encoding**. Decoder energy model: Putting it all together: **...**
Cited by 89 - Related articles - Web Search - All 8 versions

**Instruction encoding** techniques for area minimization of **instruction** ROM
T Okuma, H Tomiyama, A Inoue, E Fajar, H Yasuura - Proceedings of the 11th international symposium on System ..., 1998 - portal.acm.org
**...** The idea of such **encoding** is not entirely new. **...** It is necessary to insert a decoder
between the **instruction** memory and the **instruction register**,, named an **...**
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Cycle-accurate energy consumption measurement and analysis: Case study of ARM7TDMI- ▶uci.edu [PDF]
N Chang, K Kim, HG Lee - Low Power Electronics and Design, 2000. ISLPED'00. ..., 2000 - ieeexplore.ieee.org
**...** sys- tems saves power consumption by changing energy-sensitive fac- tors such as
**instruction** fetch addresses, opcode **encoding**, **register encoding**, data fetch **...**
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[PDF] ▶Low-power **instruction encoding** techniques
S Woo, J Yoon, J Kim, S San, K Seoul - SOC Design Conference, 2001 - davinci.snu.ac.kr
**...** The low-power **encoding** techniques are applied into the opcode, **register**
fields, and unused bit fields of an **instruction** format. **...**
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Support for garbage collection at every **instruction** in a Java compiler- ▶cmu.edu [PS]
JM Stichnoth, GY Lueh, M Cierniak - Proceedings of the ACM SIGPLAN 1999 conference on ..., 1999 - portal.acm.org
**...** frequencies, we construct a Huffman **encoding**, rather than always using three bits
per **instruction**. Figure 3 shows the distribution of **register** liveness changes **...**
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Processor utilizing a template field for **encoding instruction** sequences in a wide-word format
JM Hull, K Fielden, H Mulden, H Sharangpani - US Patent 5,922,065, 1999 - Google Patents
**...** & Zafman, LLP [57] ABSTRACT A processor having a large **register** file utilizes a
template field for **encoding** a set of most useful **instruction** sequences in a **...**
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Opcode **encoding** for low-power **instruction** fetch
S Kim, J Kim - Electronics Letters, 1999 - ieeexplore.ieee.org
**...** Low-power opcode **encoding**: When a new **instruction** is fetched into the **instruction**
**register** (IR), many bit positions of the current IR are switched to the **...**
Cited by 9 - Related articles - Web Search - All 3 versions

[PDF] ▶Xtensa: A configurable and extensible processor
RE Gonzalez - IEEE micro, 2000 - cse.ucsd.edu
**...** the mnemonic and **encoding** of a new **instruction** called BYTESWAP . The state decla-
rations define two new state registers: a single- bit control **register** ( SWAP **...**

[PDF] The test access port and boundary scan architecture
CM Maunder, RE Tulloss - 1991 - owlnet.rice.edu
... see Chapter 5). 4.4.2: **Instruction Register** Operation Figure ... involved in loading a new **instruction** into the ... 4-8 and summarized in hexadecimal **encoding** in Table ...


Key authors: **J Huang** - **J Van Praet** - **D Burger** - **R Mehta** - **T Austin**

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